In the Specification

Applicant presents replacement paragraphs below indicating the changes with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Please replace the paragraph beginning at page 2, line 29 with the amended paragraph/line as follows:

Fig. 3 illustrates, in a timing diagram, a second conventional example of control of thyristors of a composite bridge. In this case, the control is a pulse control. Control circuit [[9]] 7 provides, permanently, a pulse train (illustrated in Fig. 3) having a pulsewidth provided to ensure a sufficient conduction (a current greater than the thyristor latching current) before the pulse disappears. Referring to the example of Fig. 2, that is, in a first halfwave of rectified A.C. voltage Vinr where a crossing of curves Vout and Vinr occurs again at a time t1, the triggering (closing of thyristor TH1 or TH2) is not necessarily instantaneous. In the example shown, time t1 is subsequent to a pulse and the beginning of the next current pulse Imp1 must thus be awaited to trigger the thyristor closing. As in Fig. 2, the second halfwave of curve Vinr illustrates the case of an increase in the load supplied by the rectifying bridge. Here again, pulse Imp2 triggering the closing of one of the thyristors may be subsequent to time t2. The maximum interval between the time when curves Vout and Vinr cross and the thyristor closing is conditioned by the pulse frequency.

Please replace the paragraph beginning at page 8, line 11 with the amended paragraph/line as follows:

This turning-on of switch K causes the triggering of thyristor TH by the flowing of a gate current provided by current source 10. As soon as current I running through thryistor TH (Fig. 5D) becomes ~~smaller~~ greater than the threshold set by voltage reference Vref2, the output of comparator 131 switches and provides a high state at the reset input (Fig. 5E) of flip-flop 11 (time t3). This state switching resets output signal O of lip-flop 11 and accordingly turns off switch K.

Please replace the paragraph beginning at page 9, line 26 with the amended paragraph/line as follows:

According to an alternative embodiment not shown, comparator [[21]] 121 (or flip-flop 11) may be used to apply an external control signal (for example, a start-up signal). For example, input S of the flip-flop may receive a logic combination (for example, by an AND gate) of the output of comparator 121 and of an external start-up logic signal.